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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,515	FLOMAN ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,9 and 11-21* is/are rejected.

7)☒ Claim(s) *6,7 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

1. Claims 1-21 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 01 July 2005. The information disclosed therein has been considered.

Specification

3. Claims 18, 20 and 21 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Specifically, claims 18, 20 and 21 fail to further limit the circuit of claim 14.

4. Claims 2, 6 and 14 are objected to because of the following informalities:

In claim 2, line 2, "terminal" is understood as --terminals--.

In claim 6, a step is not clearly recited; "the two parts" is understood as --providing the two parts--.

In claim 14, line 5, "terminal" is understood as --terminals--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 8, 9 and 11-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("Admission") in view of Dent (U.S. Pat. No. 5,657,288) and Ooishi (U.S. Pat. No. 5,517,459).

Regarding claims 1 and 14, Admission, in Fig. 1, discloses a dynamic random access memory (the first paragraph on page 10 of the instant specification) and a corresponding method of addressing the dynamic random access memory, with providing a row address (R in Fig. 1) and a column address (C) to addressing terminals of the memory (inherent), in intervals provided by a timing clock signal (clock in Fig. 1).

Admission does not disclose dividing the row address and/or the column address into parts, and providing the respective parts to the address terminals at a rising edge and a falling edge of the timing clock signal.

Dent, for example in Fig. 4, discloses dividing an address into parts (the plurality of address segments, represented by the address segment registers 409 in Fig. 4), with corresponding reduction in address terminals (see for example column 3, lines 27-30).

Ooishi, for example in Figs. 18-20, discloses dividing an address into parts (for example A0(1) - A3(1) in Fig. 19) and providing the respective parts to an address terminal (Add in Figs. 18-20) at a rising edge (for example T3) and a falling edge (for example T5) of a timing clock

signal (CLK) (see also Figs. 3 and 4 for another embodiment using both the rising and falling edges of the clock).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to divide the row address and the column address of Admission into parts (as in Dent and Ooishi) and providing the respective parts to the reduced address terminals at a rising edge and a falling edge of its timing clock signal (as in Ooishi), for the purpose of efficiently processing the divided address information and reducing the overall size of the memory (due to reduction in address terminals and address lines), as well as reducing power consumption and decreasing the time required in addressing a large memory (see for example Dent column 3, lines 27-35).

Regarding claims 2, 11-13 and 15-17, the above combination further discloses that the respective parts are provided to the address terminals at consecutive rising and falling edges of the timing clock signal (see the address parts A0(1)-A3(1) in Fig. 19 of Ooishi provided at the consecutive rising and falling edges T3-T9, as applied to the above combination);

providing a latency of two rising edges for processing the column address (see the latency comprising two rising edges between C and the first D in Fig. 1 of Admission, as applied to the above combination);

processing the parts of the row address and/or the parts of the column address provided sequentially at the address terminals within the memory (see Fig. 19 of Ooishi, as applied to the above combination);

processing parts of the row address within the memory before receiving the complete row address (see Fig. 20 of Ooishi, wherein parts of an address a0(1)-a0(m) are processed by 1701 and 1711 before the complete address add0 is received, as applied to the above combination);

providing row data (i.e., the data associated with the row address) to a row buffer (for example, AB in Fig. 18 of Ooishi, as applied to the above combination) after the row address has been received (via for example 1711 in Fig. 20 of Ooishi, as applied to the above combination);

a number of address terminals T (the width of 425 in Fig. 4 and column 9, lines 43-53 of Dent, as applied to the above combination) is the address bus size ADR (the width of the full address 407 in Fig. 4 and column 9, lines 43-53 of Dent, as applied to the above combination) divided by N, such that T = |ADR/N|, where N is the number of parts for the row address and/or the column address (the number of 409 in Fig. 4 and column 9, lines 43-53 of Dent, as applied to the above combination).

Regarding claims 3, 5 and 8, the above combination discloses a method of claim 1 or 14, with the exception of dividing the row address into two parts; dividing the column address into two parts; or dividing the row and/or the column address into more than two parts.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to divide the row address and the column address of the above combination respectively into two parts or more than two parts, since discovering the optimum or workable ranges, or an optimum value of a result effective variable (i.e., the number of parts in the row address and/or the column address and thus the number of address terminals) involves only routine skill in the art.

Regarding claims 4 and 9, the above combination further discloses providing the two parts of the row address, respectively, at a first rising edge and a first falling edge within a timing cycle of the timing clock signal (i.e., the first consecutive rising and falling edges, with reference to Ooishi Fig. 19 and claim 2 above, as applied to the above combination);

providing the parts of the row address at rising and falling edges at the beginning of a timing cycle of the timing clock signal, respectively (see Fig. 1 of Admission and Fig. 19 of Ooishi, as applied to the above combination).

Regarding claim 18, the above combination further discloses a computer system comprising a central processing unit (see for example CPU 31 in Fig. 3a of Dent) and a memory device (RAM 32 in Fig. 3a of Dent), in particular according to claim 14 (the memory device of the above combination), with an address bus providing row address and column address from the central processing unit to the memory device sequentially (see Figs. 3a and 4 of Dent, and Figs. 4 and 19 of Ooishi, as applied to the above combination), a clocking device providing a timing clock signal with rising and falling edges (for example, CLK of Ooishi), characterised by address processing means dividing the row address and/or the column address in parts, and providing the respective parts to address terminals of the memory device at rising and falling edges of the timing clock signal (as in claims 1 and 14 above).

Regarding claim 19, the above combination further discloses a computer program product (see for example Figs. 2 and 3a of Dent) with a computer program (within 20 or 30 in Figs. 2 and

3a of Dent) stored thereon for providing address information to a memory device for accessing data within the memory device (see also Dent column 1, lines 7-35), the program comprising instructions operable to cause a processor to, provide a row address and a column address to addressing terminals of the memory device sequentially, characterised by dividing the row address and/or the column address into parts, and providing the respective parts to the address terminals at a rising and a falling edge of a clock signal (as in claims 1 and 14 above).

Regarding claims 20 and 21, the above combination further discloses a use of a memory device of claim 14 in consumer electronic devices or mobile communication devices; or a mobile communication device comprising a memory device of claim 14 (see for example Dent column 1, lines 7-35, as applied to the above combination).

Allowable Subject Matter

7. Claims 6, 7 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 6 and 10, the prior arts of record do not disclose or suggest a method as recited in claim 6 or 10, and particularly, providing the two parts of the column address, respectively, after a latency time for processing the row address at a first falling edge and a following rising edge within a timing cycle of the timing clock signal; or providing the parts of

the column address after a latency time for processing the row address at the falling and rising edges at the end of a timing cycle of the timing clock signal, respectively.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Garner (U.S. Pat. No. 5,428,770); Hardee et al. (U.S. Pat. No. 5,077,693); Jones et al. (U.S. Pat. No. 5,815,510)

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

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